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AF/2187

PATENT APPLICATION

ATTORNEY DOCKET NO. 10016630-1

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Terry Lyon

Confirmation No.: 3380

Application No.: 10/071,069

Examiner: K. McLean Mayo

Filing Date: Feb. 8, 2002

Group Art Unit: 2187

Title: MULTILEVEL CACHE SYSTEM HAVING UNIFIED CACHE TAG MEMORY

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PO Box 1450
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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on Mar. 5, 2004.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $330.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$420.00
( )	three months	$950.00
( )	four months	$1480.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$330.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: May 4, 2004

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Respectfully submitted,

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PATENT
Attorney Docket No. 10016630-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Lyon
Serial No.:	10 071,069
Filed:	02/08/2002
Group Art Unit:	2187
Examiner:	Kimberly McLean Mayo
For:	Multilevel Cache System Having Unified Cache Tag Memory

BRIEF

PURSUANT TO 37 C.F.R. § 1.192

I. Real Party in Interest

The real party in interest for this appeal is Hewlett-Packard Development Company, L.P. (HPDC), a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, L.L.C. Evidence of this assignment, which was recorded on December 2, 2003, may be found at reel/frame 014177/0428.

II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1–13 stand rejected, and are pending for consideration in this appeal.

IV. Status of Amendments

No amendments to the claims have been filed subsequent to the Final Office Action issued on 12/05/2003, i.e., there are no pending amendments.

V. Summary of the Invention

The following summary is an edited excerpt based on the Summary of the Invention section in Appellant's specification, paragraph numbers 21, 22, and 24:

A computer system is disclosed that has more than one level of cache, and which, in one embodiment, includes three levels of cache. Two of these levels of cache are implemented in a hybrid cache system. The hybrid cache system has a unified cache tag subsystem, common to both of its cache levels. The unified cache tag subsystem has at least one way of associativity. Each way of associativity has associated address, level, and flag fields. The address field is used to determine whether a "hit" occurs, and the level field indicates a lower level cache "hit" and in which "way" of storage the hit is located.

In one embodiment, there are two levels of cache. Both of these levels of cache are implemented in a hybrid cache system having a unified cache tag subsystem.

VI. Issues

1. *Whether* Steely *fails to teach or suggest every element recited in Appellant's independent claims 1, 7, and 13, and is therefore not anticipatory art under 35 U.S.C. sec. 102.*

2. *Whether the Examiner's modification of the Steely reference is proper, and whether the reference is modifiable, or operable when modified, to yield the claimed invention.*

3. *Whether* Steely *teaches away from Appellant's claimed invention, and therefore tends to show nonobviousness of the invention.*

VII. Grouping of Claims

Group I: Claims 1– 13 stand together.

VIII. Argument

A. REASONS FOR ALLOWABILITY OF THE CLAIMS

1. Steely fails to teach or suggest every element recited in Appellant's independent claims 1, 7, and 13, and is therefore not anticipatory art under 35 U.S.C. 102.

In the Final Office Action, claims 1-3, 6-8, 10-11, and 13 (including independent claims 1, 7, and 13) were rejected under 35 U.S.C. sec.103(a) as being anticipated by Steely, PGPUB US 2002/0099913 A1.

However, Steely fails to teach or suggest the unified cache tag element recited in each of the independent claims 1, 7, and 13, more specifically, the "unified tag memory" 312 recited in Appellant's claim 1, and the "unified tag subsystem" 214 recited in claims 7 and 13.

The hybrid cache system recited in each independent claim has a *unified* cache tag subsystem 214, common to both of its cache levels [Appellant's specification, paragraph 22]. The cache tag memory 214 [Figure 2] is *unified* in that each location in unified cache tag memory 312 [Figure 3] contains information for locating data in both second level data cache 212 and third level data cache 216. In addition, each read of cache tag memory 214 simultaneously reads information for locating data in second level data cache 212 and third level data cache 216 [Appellant's specification, paragraph 34].

The concept of a 'unified tag' is thus defined in the specification. Noting that an inventor is entitled to be his own lexicographer in accordance with well-established principles of patent law, the terms "unified tag memory" and "unified tag subsystem" are therefore sufficiently well-defined, and their inclusion as an element in each of Appellant's independent claims distinguishes the system claimed therein from Steely's teachings.

In at least one important aspect, the *unified* cache tag system of the present invention differs from the cache tag system described in Steely, in that Steely specifically states that "each cache level includes a tag store"; [Steely, paragraph 15, line 8]. By virtue of this statement, Steely clearly does not contemplate the presently claimed 'unified cache tag', since the present invention unified tag memory 214 is a singular, unified, tag store ***shared*** by at least ***two*** levels of cache.

Appellant's "unified cache tag" uses a *unified* cache tag technique, wherein *each* tag address in tag memory 312, and further each tag address comparator

320, is used to index *two* or more distinct *levels* of cache data memory 212, 216 [Appellant's specification, paragraph 34, 36-38 and Figures 2 and 3, reference numbers 214, 312, 320, 342, 336, 347, 340, 349]; this technique permits the present system as described and as claimed to, among other things, avoid Steely's step 732 for references by a processor to the lower of the two levels of cache 212, 216 addressed by the unified tag subsystem 214. To summarize, an important distinction between Steely's teachings and all claims in the present application is that Steely's system has separate tag systems for each cache level, and this multiplicity of cache tag systems are not *unified*, in that *each* tag address and tag address comparator of Steely is used to index only *one level* of cache.

Steely also fails to provide the unified tag memory coupled to provide valid flag identification information to hit-logic units of two levels of cache, as recited in Appellant's independent claims 1, 7, and 13. Appellant's claims require that each cache tag have associated upper 360 and lower 332 level valid flags. These valid flags indicate presence of *valid* data in their respective associated cache data memory locations 212, 216, and drive separate hit logics 336, 340, for each of upper and lower cache levels. Each valid flag 360, 332 is 'AND'-ed [342] with output of the way-specific address comparator 320 and coupled to *both* hit logics 336, 340 [Appellant's specification, paragraph 37-40, drawing reference numbers 312, 332, 360, and claims 1, 7, and 13]. This commonality is lacking in Steely.

While the inval_miss flag of Steely's lower level cache provides some information about upper level cache contents, Steely differs fundamentally from Applicant's claimed device. In Steely, if no cache hit is found in low level cache, the inval_missflag in low level tag memory is unavailable because his inval_missflag is meaningful only with matching cache tags. Since an unmatched inval_mis flag cannot indicate valid data in upper level cache; determining presence of data in Steelys upper level cache requires a lookup in Steelys upper level cache tag store. Steely therefore does not provide upper and lower valid flags in the same tag memory.

Steely does not provide a *unified* tag memory coupled to provide cache tags to a singular comparator, the comparator in turn providing cache hit information to hit-logic units of two levels of cache, as recited in Appellant's independent claims,

because nowhere in Steely (or in the other cited art) is it suggested that the tag address [Appellant's Figure 3, reference number 360] and comparator [320] can be shared between multiple levels of cache data memory.

Note that Steely describes his Figure 3 in paragraph 21 as "a highly schematic block diagram of *a cache level* of the computer system of Fig. 1" [emphasis added].

In order to provide the singular tag memory element [Appellant's Figure 3, reference number 312] coupled to provide way identification to hit logic units [Figure 3, nos. 336, 340] of two levels of cache, as recited in Appellant's claims 1, 7, and 13, the Examiner has drawn a sweeping stroke through multiple levels of a complex system, arbitrarily combining an address field of a lower level tag store (Steely 304, copy from lower level tag system 206) and an address field of an upper level tag store (Steely 304, copy from upper level tag system 208) into a unified tag store. Absent a requirement (unstated in Steely) that addresses to each *separate copy* of tag store (Steely 304) are always the same, merging these memories into a single memory would not be feasible for several reasons, including:

a. with N (the number of address lines of lower level tag store) plus M (the number of address lines of upper level tag store), the total address lines to the array becomes impracticably huge, if N and M are each 14, representing a reasonable 16K locations in each tag memory, the sum is 28, implying 256 million locations in a merged memory,

b. each time lower level tag store location A is written, it would be necessary to effectively write 16K locations – the locations determined by combining vector A with all possible upper level tag store addresses – with the new data, and

c. such a large memory would be too slow to be practical.

The Examiner has also drawn a bold stroke through the "lowest cache level" [Steely, paragraph 38, line 1] and the "next higher cache level" [Steely, paragraph 39, line 7] to merge the comparators cited by the Examiner (as Steely paragraph

38, lines 7-10 and paragraph 39, lines 6-14) into Appellant's way-specific comparator 320.

A primary reason for implementing Appellant's claimed invention is to reduce memory size by requiring that only one set of address tags and one set of tag comparators to address both levels of cache. Steely thus actually teaches away from the structural simplicity of Appellant's claimed invention by describing separate tag memory and comparators in each cache level.

Therefore, for at least the above reasons, the Steely reference is not anticipatory art under 35 U.S.C. 102, since the reference fails to teach or suggest every element of Appellant's invention, as recited in each one of the independent claims 1, 7, and 13.

2. The Examiner's modification of the Steely reference is improper, and the reference is not modifiable, or operable when modified, to yield the claimed invention.

a. *There is no suggestion or teaching to be found, either in the cited references, or in the prior art, to modify the system disclosed in* Steely *to combine two sub-tags to form a 'unified' tag, nor is there a suggestion or teaching to modify the Steely system to combine two comparators to form a "unified" comparator.*

Appellant believes that the Examiner has impermissibly modified the Steely reference by combining two different sub-tags and two different comparators disclosed therein, which modification is neither taught nor suggested by the reference, and thus cannot be used as prior art to reject any of Appellant's claims.

In rejecting independent claims 1, 7, and 13, the Examiner stated, in paragraph 3 of the Final Office Action, that:

> "Regarding claim1, Steely discloses a unified tag memory coupled to be addressed by the tag index portion of the tag line address, the tag memory comprising at least one way specific address tag (Figure 3, comprised of sub-tags Reference 304 in Figure 3 for the L1 and the L2 cache)..." [emphasis supplied].

Similarly, the Examiner stated in paragraph 3:

> ...at least one first comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match (the first comparator is comprised of the compared function refereed to on Page 4, section [0038], lines 7-10; and the comparing function referred to on Page 4, Section [0039], lines 6-14 – comparing function is performed by comparator(s), ...

However, Appellant asserts that the Steely reference cannot be modified this fundamentally, absent some specific motivation or suggestion found in the prior art. To cite, as prior art, the case where the two sub-tags are combined, would require proper support for the combination of the sub-tags for the L1 and the L2 cache, and the comparators for the L1 and L2 cache. Such a combination cannot be properly made based on Steely, since the Steely reference discloses the "two sub-tags" and the comparators as distinct entities which are fundamentally not combinable in accordance with any aspect of Steely's teachings.

Since the Examiner does not explicitly show where in the reference or in the prior art any bona fide motivation for modifying the reference may be found, Appellant asserts that such motivation can be found only in Appellant's disclosure, and therefore the modification of the references is improper, and cannot be used as a basis for showing either anticipation or obviousness of Appellant's claims. The requirement that the motivation to combine isolated elements must be found in the prior art, apart from Appellant's disclosure, is well established by the case law:

> ... the record must provide a teaching, suggestion, or reason to substitute [element A] for [element B] in the prior art. **The absence of such a suggestion to combine is dispositive in an obviousness determination** [emphasis supplied]. See SmithKline Diagnostics, Inc. v. Helena Lab. Corp., 859 F.2d 878, 886-87, 8 USPQ2d 1468, 1475 (Fed. Cir. 1988). *Gambro Lundia Ab V. Baxter Healthcare Corporation* (Fed. Cir. 1997)

For this reason alone, each claim rejection based on the Steely reference, as modified by the Examiner, must fail, since these rejections are based on a modification of the reference, which is impermissible because the Examiner has failed to show the source of any motivation, other than Appellant's specification, to make the Examiner's proposed modification of the cited reference. Since each rejection in the Final Office Action uses the Steely reference as a basis for the rejection, all rejections must fail, since Steely, as indicated herein, neither teaches

nor suggests one or more elements of Appellant's invention as claimed in each of the independent claims 1, 7, and 13.

"The mere fact that the references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" [M.P.E.P. 2143.01]. The present Office Action is devoid of any indication that would show *where* in the reference itself any such suggestion to modify the system of Steely can be found.

In a nutshell, there is nothing to be found, either in the Steely reference or anywhere in the other cited art, that teaches or suggests modifying the teaching of Steely by combining tags for two different cache levels into a single, unified, cache tag memory (i.e., the sub-tags for the L1 and the L2 cache in Steely), let alone entering each tag address only once. Since there has been no showing, either in the cited art, or in the prior art in general, of any motivation to make the modification proposed by the Examiner, Appellant maintains that no proper basis for rejection of any of the independent or dependent claims has been established.

b. *The Steely reference is not modifiable, per the Examiner's indicated combination of elements, to yield the claimed invention.*

One could not, practically speaking, combine Steely's sub-tags for the L1 and the L2 cache to yield Appellant's system, since the system described therein would not be capable of functioning in accordance with Appellant's invention as claimed in each of the independent claims because of the exponential size increase of combined memories as described above, absent a requirement that both sub-tag memories have the same addresses at all times. This fundamental incompatibility between the teaching of Steely and Appellant's claimed invention is highly indicative, if not dispositive, of the fact that the combinability of these two claimed elements *cannot be suggested* by the references. Appellant maintains that one skilled in any relevant art would not be motivated to combine two or more things that are not inherently combinable.

The Final Office Action misses the point(s) that the prior art must not only provide the basis or suggestion to effect the result indicated by the Examiner, but also that the cited reference itself must be capable of being modified to reach the

claimed end result. Therefore, for at least the above reasons, Appellant maintains that none of the claims in the present application have been shown to be anticipated by or obvious over the Steely reference.

3. ***The primary reference, Steely, teaches away from Appellant's claimed invention, and therefore, the reference tends to show nonobviousness of the invention and thus cannot be used to establish a prima facie case of obviousness.***

Nothing in Steely, or in the other cited art, provides a suggestion that a singular tag memory is capable of providing this information for more than the hit-logic unit of a single level of cache, so rejection under 35 U.S.C. 103 over Steely, in view of any presently applied reference, is not appropriate. Steely, in fact, teaches away from a singular tag memory, because Steely explicitly states that "each cache level includes a tag store" [Steeley, paragraph 15, line 8]; while Appellant's claimed invention uses a fundamentally different unified tag memory to access two levels of cache.

Steeley also teaches away from Appellant's device because his "inval_miss" flag in a lower level cache, that indicates data is *not* valid in higher level cache. Steeley's "inval_miss" flag distinguishes between the possible conditions of 'data MAY (but need not) be present in upper level cache', and 'data at this point in upper level cache is known not valid'. Steeley also has a valid flag in the lower level cache. A cache system having valid and "inval_miss" flags as described in Steeley, requires (when valid=0 and inval_miss=0) access to upper level tag memory to determine whether data is present in upper level cache, and is thus indicative of the fact that Steely's teaching heads in a fundamentally different direction from that of Appellant's claimed invention.

B. Grouping of Claims

The claims in Group I stand or fall together.

IX. Conclusion

The Steely reference forms a basis for the rejection of each of Appellant's claims in the final action of record. Because Appellant has shown that the Steely reference is deficient with respect to teaching or

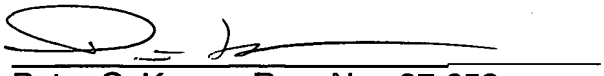
suggesting at least one element (e.g., a unified cache tag) in each of Appellant's independent claims, every rejection of these claims must therefore fail, whether based on 35 U.S.C. sec.102 *or* sec. 103, in view of the fact that this element, at least, is not provided by any of the cited references.

Allowability of the independent claims dictates that each of the dependent claims is also allowable by virtue of inherency. Therefore, Appellant believes that dependent claims 2–6 and 8–12 are also allowable, since each of these claims depends from an allowable independent claim.

Appellant therefore believes that all pending claims are allowable over the cited art because, *inter alia*, the present Office Action fails to establish a *prima facie* case of unpatentability for any of the claims. Such a *prima facie* case is non-existent because, among other things, (1) there is no prior art presented that individually or cumulatively teaches or suggests each of the elements of any of Appellant's claims, and (2) no proper motivation is provided to modify the teachings of the Steely reference. During patent examination the PTO bears the initial burden of presenting a *prima facie* case of unpatentability. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If the PTO fails to meet this burden, then the applicant is entitled to the patent. *In re Glaug*, 62 USPQ2d 1151 (Fed. Cir. 2002).

Appellant believes that claims 1–13 fully comply with 35 U.S.C. § 112 and, for at least the above reasons, are not obvious in view of the cited art to one skilled in the art having knowledge thereof. Accordingly, Appellant respectfully submits that claims 1–13 are patentable over the prior art and respectfully requests this Board to so indicate.

Respectfully submitted,



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X. APPENDIX OF CLAIMS ON APPEAL

1. (Amended) A unified tag subsystem for a multilevel cache memory system having an upper level and a lower level of cache data memory, the tag subsystem having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part, the unified tag subsystem comprising:

a unified tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag, at least one upper level valid flag, and at least one way-specific lower level flag;

at least one first comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match, and the lower level flag of the tag memory indicates a valid entry in the lower cache; and

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and a high level valid flag of the tag memory is in a valid state.

2. (Original) The unified cache tag subsystem of Claim 1, wherein there are at least two way-specific address tags, and at least two first comparators.

3. (Original) The unified cache tag subsystem of Claim 2 wherein the unified cache tag subsystem further comprises cache coherency maintenance logic coupled to the tag memory subsystem.

4. (Original) The unified cache tag subsystem of Claim 3, wherein the coherency maintenance logic is cache snoop logic.

5. (Original) The unified cache tag subsystem of Claim 1 wherein the at least one way-specific lower level flag comprises information

indicating a way of storage in lower level data memory at which cache data may be located.

6. (Original) The unified cache tag subsystem of Claim 5, wherein there are a plurality of first comparators for multiple ways of associativity.

7. (Original) A multilevel cache memory system having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part; the multilevel cache memory system comprising:

a lower level cache data memory coupled to provide data to the processor port on a lower level cache hit;

an upper level cache data memory coupled to provide data to the processor port on an upper level cache hit;

a unified tag subsystem further comprising:

a tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag field, at least one way-specific lower level flag field, and at least one way-specific upper level valid flag;

at least one comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the lower level flag indicates valid cache data in the lower level cache data memory; and

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and the a higher level valid flag field indicates valid cache data in a upper level cache data memory.

8. (Original) The cache system of Claim 7, wherein the higher level valid flag field comprises a plurality of higher level valid flags, and wherein each higher level valid flag indicates validity of data in a line of a superline in upper level cache data memory.

9. (Original) The multilevel cache memory system of Claim 7 wherein a cache line of the lower level cache data memory is smaller than a cache line of the upper level cache data memory, wherein lower level cache data memory has fewer ways of storage than the upper level cache data memory, wherein the lower level flag field of the unified cache tag subsystem further comprises a plurality of lower level flags, wherein the lower level flags indicate ways of storage in lower level cache data memory where corresponding data is located in lower level cache data memory.

10. (Original) The multilevel cache memory system of Claim 7, wherein the multilevel cache memory system further comprises cache coherency maintenance logic.

11. (Original) The multilevel cache memory system of Claim 7, wherein the upper level valid flags of the cache tag memory subsystem further comprise a plurality of way-specific superline segment valid flags, and wherein each superline segment valid flag contains validity information for an upper level cache line of an upper level cache superline, and wherein the upper level cache data memory is capable of storing a plurality of superlines.

12. (Original) The multilevel cache memory system of Claim 7, wherein the unified tag subsystem further comprises way limit apparatus whereby specific ways of storage may be disabled.

13. (Amended) A multilevel cache memory system having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part; the multilevel cache memory system comprising:

a lower level cache data memory coupled to provide data to the processor port on a lower level cache hit;

an upper level cache data memory coupled to provide data to the processor port on an upper level cache hit;

a unified tag subsystem further comprising:

a tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag field, at least one way-specific lower level flag field, and at least one way-specific upper level valid flag;

at least one comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the lower level flag indicates valid cache data in the lower level cache data memory;

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and the a higher level valid flag field indicates valid cache data in a upper level cache data memory; and

wherein the upper level data cache is larger and slower than the lower level data cache.